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AI for New Devices And Technologies at the Edge

D4.4 Design, test and evaluation of the Mixed-signak SNN ASICs V2

Deliverable No.	D4.4	**Due Date**	*29-Feb-2024*
Type	Report	**Dissemination Level**	*Confidential*
Version	1.5	**Status**	Final
Description	This V2 describes the characterization of SynSense ASIC 1.3 a mixed signal audio encoding front-end designed to enable efficient audio processing with SNNs. It also describes simulation results of the UZH ASIC 1.2 always-on SNN core, the first samples are expected in Q2/2024.		
Work Package	WP4 – Implementation of ICs and Platforms.		

Abstract (Published Summary)

ANDANTE's overarching goal is to leverage innovative hardware accelerators and related platforms for Artificial Neural Networks (ANN) and spiking neural networks (SNN) as a basis for future products in the IoT Edge domain.

The objective of WP4 “Implementation of integrated circuits and platforms” is the development of ASICs and neuromorphic platforms, based on the use cases and system requirements defined in WP1 “Use Case System Architectures Description and Application Requirements” and implemented in WP5 “Applications Integration, Validation and Evaluation”.

Task 4.1 concerns the design and implementation of mixed-signal SNN accelerator ASICs. In this deliverable describes:

- The characterization of a mixed-signal audio coding front-end, ASIC1.3, is designed to enable efficient audio processing with SNNs. This design was described in detail in D4.3 and features a “Xylo” ASIC from partner SynSense, including the mixed-signal audio front-end and a digital SNN inference core. This deliverable D4.4 describes the test procedure and characterization results for multiple Xylo devices.
- The specifications, design details, simulation results, and preparations for measurements of ASIC 1.2. The SNN processor developed by UZH incorporates efficient on-chip learning, dynamic sparse training, and a mixed-timing design. This processor is versatile, making it a prime candidate for in-sensor or near-sensor computing. Its efficient on-chip learning allows it to adapt to changes in the environment and user behavior. The dynamic sparse training feature facilitates evolutionary sparse neural network (NN) training directly on the chip, crucial for minimizing reliance on external memory for storing NN parameters. The mixed-timing design, which does not rely on clock signal sampling for input events, aligns well with event-driven computing and conserves energy during idle periods, essential for devices intended to be always on. The processor's flexibility in configuration allows it to be tailored to various topologies and NN sizes, enabling users to optimize performance and energy efficiency for different tasks.