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ANDANTE

AI for New Devices And Technologies at the Edge

D4.3 Architecture design of the ASICs

Deliverable No.	D4.3	**Due Date**	*01-Nov-2021*
Type	Report	**Dissemination Level**	*Confidential*
Version	1.0	**Status**	Final
Description	This deliverable provides an overview of the architecture of WP4 ASICs and SoCs as well as their implantation specification.		
Work Package	WP4 – Implementation of ICs and Platforms.		

Abstract (Published Summary)

The overarching goal of ANDANTE is to leverage innovative hardware accelerators and associated platforms for Artificial Neural Networks (ANN) and Spiking Neural Networks (SNN) as a basis for future products in the Edge IoT domain.

The objective of WP4 “Implementation of ICs and Platforms” is the development of the neuromorphic ASICs and platforms, based on the use cases and system requirements defined in WP1 “Use Case System Architectures Description and Application Requirements” and implemented in WP5 “Applications Integration, Validation and Evaluation”. Moreover, WP4 ASIC developments will profit from the silicon technologies addressed in WP2 “New Memory Technologies for AI applications” as well as the HW building blocks and Foundation IPs defined by WP3 “AI Building Blocks, Methods and Tools”.

Three different tasks in WP4: Task 4.1, Task 4.2, and Task 4.3 take care of the integrated circuit designs (ASICs and SoCs) in the project. The results of these tasks are planned to be periodically reported through five deliverables: D4.1, D4.3, D4.4, D4.5 and D4.6.

D4.1 provided the specification requirements of ASICs and SoCs to be designed in WP4 while D4.3 provides the architecture overview and implementation specifications. Therefore, D4.3 provides more detailed information about the ANDANTE designs. The three last deliverables (D4.4, D4.5 and D4.6) will provide simulation results of the designs and the ASICs and SoCs characterization.

This deliverable provides a detailed overview of the different ASICs and SoCS at architecture level and indicates the targeted performances: power consumption, latency, number of quantized bits, etc. for each integrated circuit. Finally, it describes the interfaces, which form the basis for the later deployment and integration of these ICs in the custom ANDANTE platforms and boards to be used in the WP5 for the implementation of the 13 use cases addressing 5 different domains.

Table 1 lists and summarizes the neuromorphic ASICs and SoCs to be developed in ANDNATE for efficient Edge Computing Solutions.

Table 1: Technology summary of ANDANTE ASICs and SoCs

AI Component	ID	Description	Memory	Technology	Design Partner
Mixed-signal SNN	ASIC 1.1	Multi-ASIC for exploration of parallelized and distributed SNN algorithms	RRAM	28nm	Infineon
Mixed-signal SNN	ASIC 1.2	Multi-core targeting low-dimensional signal representations, such as auditory signals, vibrations, or bio-signals not related to machine vision	SRAM	180nm	University of Zurich
Audio Front-end	ASIC 1.3 Audio processing	Low -power analog audio front-end performing analog filtering via a set of tunable bandpass filters for its processing by a Spiking Neural Network.	--	40nm	SynSense
Digital MCU with AI	SoC 1.1:	SoC combining a Microcontroller STM32 microcontroller with AI		28 nm or lower	STMicro-electronics

	STM32 AI MCU	acceleration via a neural processing unit			
Digital ANN	ASIC 2.1 NeuroCorgi	Feature extractor circuit to address image classification, segmentation and detection applications	SRAM	22nm FDSOI	CEA
Digital CNN	SoC 2.1: Visage 2	Neural Compute Engine (NCE) targeting NN acceleration for smart vision applications in digital life domain	SRAM or MRAM	22nm FDSOI	CSEM
Mixed-signal ANN	ASIC 3.1: ADELIA 22 Gen2	Scalable and configurable mixed-signal inference accelerator with a multi-core architecture using analog in-memory computing. In the ANDANTE project, this ASIC is targeting voice activity detection (VAD).	SRAM	22nm FDSOI	Fraunhofer IIS&EMFT, FAU
Mixed-signal ANN	ASIC 3.1b:	Flexible SoC for convolutional neural networks integrating multiply-accumulate (MAC) accelerators using FeFETs with a RISC-V microcontroller. In the ANDATE scope, Heiman Optical Sensor data is targeted as a use case.	FeFET	28nm or lower	Fraunhofer IPMS
Mixed-signal aNN	ASIC 3.2:	Analogue neuronal network (aNN) for tinyML applications. To be evaluated in the context of color recognition.	RRAM	28nm TSMC	Infineon

Each Section of the document addresses one of the integrated circuits and follows a similar structure providing the following subsections: a motivation for the design, an overview of the top-level architecture and the general specifications. Afterwards, the implementation specifications are provided for the most relevant blocks. A subsection provides a link between the blocks designed in WP3 and used in the WP4 designs. Pinout and packaging type are also specified and in some cases floorplan and area estimation are included too.

It should be noted that the content of D4.3 compared with D4.1 has been updated an includes the current development status. Furthermore, it provides a more detailed overview of the top level and some critical blocks constituting the ASIC and SoCs architectures are highlighted. Moreover, this deliverable provides operating conditions and performance specifications for them.