

This project has received funding from the Electronic Components and Systems
for European Leadership Joint
Undertaking under grant agreement No 876925



AI for New Devices And Technologies at the Edge

D4.2 Platforms Requirements and Specifications

Deliverable No.	D4.2	Due Date	30-Jun-2021
Type	Report	Dissemination Level	Confidential
Version	1.0	Status	Final
Description	This document provides the requirements and specifications of the different platforms to be developed in the ANDANTE project based on the Artificial (ANN) and Spiking Neural Networks (SNN) ASIC accelerators. These platforms will be used by the different use cases to demonstrate the technologies developed in ANDANTE as well as their performances.		
Work Package	WP4 – Implementation of ICs and Platforms.		

PROPRIETARY RIGHTS STATEMENT

This document contains information, which is proprietary to the ANDANTE Consortium.

Neither this document nor the information contained herein shall be used, duplicated or communicated by any means to any party, in whole or in parts, except with prior written consent of the ANDANTE consortium.

Abstract (Published Summary)

The overarching goal of ANDANTE is to leverage innovative hardware platforms for artificial neural networks (ANN) and spiking neural networks (SNN) as a basis for future products in the Edge IoT domain. The objective of WP4 "Implementation of ICs and Platforms" is the implementation of the neuromorphic ASICs and platforms to cope with the use cases and system requirements defined in WP1 "Use case system Architectures description and application Requirements" and WP5 "Applications Integration, Validation and Evaluation", and using the basic technologies from WP2 "New Memory Technologies for AI applications" and the HW building blocks developed by WP3 "AI Building Blocks, Methods and Tools".

This deliverable is part of the Task 4.4 "Platforms development". It aims the following objectives:

- First, it details and complements the general requirements and decisions elaborated by WP1/2/3 and the WP4 tasks T4.1, T4.2, T4.3 for the specific needs of the different ANDANTE platforms according to their associated use cases.
- Second, it defines the design specifications of the hardware platforms and their components (others than ASICs and SoCs, which are defined in D4.1) as well as the board interfaces, which form the basis for the later implementation of these platforms. In particular four platforms and one board are planned in the project, as described in the following table:

Platform/ board	Short Description	Associated Components	Associated Domains and Use Cases	Contribut ors
4.1	STM32-based hybrid neuromorphic platform combining SNN and ANN ASICs to perform complementary and efficiently AI features. Designed to support a variety of applications in digital farming, transport and smart mobility, and digital life domains	SoC 1.1, ASIC 1.2, ASIC 1.3, ASIC 2.1	Digital Farming: UC2.1, UC2.2 Transport and Smart Mobility: UC3.1, UC3.2, UC3.3, UC3.4 Digital life: UC5.1, UC5.2	CEA, STG, SynSense, Televes, University of Zurich
4.2	A Spiking Neural Microcontroller (SNMC) platform intended, for instance, for radar/optical sensor applications	ASIC 1.1	Digital Industry: UC1.1 Healthcare: UC4.3	Infineon
4.3	Includes a mixed-signal ASIC and controller/peripheral units, suitable for instance for voice activity detection	ASIC 3.1	Digital Industry: UC1.1 Digital life: UC5.1.4	Fraunhofer
4.4	It is an off-the-shelf platform that will be used for the smart vision applications in the digital life domain. Provides effective interface between SynSense accelerator and the event-based camera with low latency and low	SoC 2.1	Digital life: UC5.2	CSEM, SynSense

	power consumption for vision-based human-computer interaction.			
Board 4.1	An Analog Neuronal Network Microcontroller (ANMC) board; only intended for the evaluation of ANN ASICs	ASIC 3.2	Digital life: UC 5.1.5	Infineon