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ANDANTE

AI for New Devices And Technologies at the Edge

D4.1 ASICs Requirements and Specifications

Deliverable No.	D4.1	**Due Date**	*01-Jul-2021*
Type	Report	**Dissemination Level**	*Confidential*
Version	1.3	**Status**	Final
Description	This deliverable provides the requirements and high level architectural specifications of the different ASICs and SoCs to be developed within ANDANTE.		
Work Package	WP4 – Implementation of ICs and Platforms.		

Abstract (Published Summary)

The overarching goal of ANDANTE is to leverage innovative hardware accelerators and associated platforms for Artificial Neural Networks (ANN) and Spiking Neural Networks (SNN) as a basis for future products in the Edge IoT domain. The objective of WP4 "Implementation of ICs and Platforms" is the development of the neuromorphic ASICs and platforms, based on the **use cases** and system requirements defined in WP1 "Use Case System Architectures Description and Application Requirements" and implemented in WP5 "Applications Integration, Validation and Evaluation". Moreover, WP4 ASIC developments will be also considered the silicon technologies addressed in WP2 "New Memory Technologies for AI applications" as well as the HW building blocks and Foundation IPs defined by WP3 "AI Building Blocks, Methods and Tools".

This deliverable is part of tasks 4.1, 4.2 and 4.3 of WP4, which target the implementation of several ASICs and the development of SoC architectures. First, it details and complements the general requirements and decisions elaborated in mentioned WP1, WP2 and WP3. Second, the deliverable defines the architecture and indicates the targeted performances (power consumption, area, etc.) for each ASIC and SoC. Finally, it describes the interfaces, which form the basis for the later implementation and integration of these devices in the custom ANDANTE platforms/boards to be used in the use cases in WP5.

The following Table lists the neuromorphic ASICs and SoCs for Edge Computing Solutions

AI Components	ANDANTE ID	Description	Techo	Design Owner
Mixed-signal SNN	ASIC 1.1	Multi-ASIC for exploration of parallelized and distributed SNN algorithms	28 nm CMOS	Infineon
Mixed-signal SNN	ASIC 1.2	Multi-core targeting low-dimensional signal representations, such as auditory signals, vibrations, or bio-signals not related to machine vision	28 nm FDSOI	University of Zurich
Front-end	ASIC 1.3	Audio front-end performing acoustic inference sensing tasks: acoustic feature extraction (AFE) and classification	40 nm	SynSense
Digital ANN	ASIC 2.1	Feature extractor circuit to address image classification, segmentation and detection applications	22nm FDX	CEA
Digital CNN	SoC 2.1	Neural Compute Engine (NCE) targeting NN acceleration for smart vision applications in digital life domain	22nm FDX	CSEM
Mixed-signal ANN	ASIC 3.1	Inference accelerator with a multi-core architecture using analog in-memory computing; targeting voice activity detection (VAD)	22nm FDX	Fraunhofer
Mixed-signal ANN	ASIC 3.2	Analogue neuronal network (aNN) for tinyML applications. To be evaluated in	28nm CMOS	Infineon

AI Components	ANDANTE ID	Description	Techo	Design Owner
		the context of one-key-word-spotting for a limited amount of accents	with RRAM	
Digital MCU with AI	SoC 1.1	Microcontroller STM32 aiming to identify best tradeoff between SoC features and functionality, having a direct impact on the silicon area and final cost	28 nm or lower	STGNB