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ANDANTE

AI for New Devices And Technologies at the Edge

D3.9 Low TRL Technology Foundation IPs implementation

Deliverable No.	D3.9	**Due Date**	*31-Dec-2022*
Type	Report	**Dissemination Level**	*Confidential*
Version	1.0	**Status**	Final
Description	This deliverable reports the design of three low TRL IPs developed within Task 3.4. These IPs are fundamental subcircuits implementing 3 different IP designs of Analog in Memory Computing (AiMC) function based on emerging NVM technologies developed in WP2. Each IP is described separately. It should be noted that in ANDANTE, several eNVM technologies are being developed and different design approaches are being explored.		
Work Package	WP3 – AI building blocks, Methods and Tools.		

Abstract (Published Summary)

This deliverable aims at presenting the low TRL Foundation IPs developed in task 3.4. These Foundation IPs really compose a key point of the ANDANTE project as they form a link between the emerging NVM technologies, and the neuromorphic architectures designed in WP4. As memory access consumes an important part of the energy in neuromorphic applications and as the number of parameters becomes larger and larger, the density and power efficiency of these IPs have a major impact on the overall efficiency of ICs where they are used and on the success of ANDANTE project.

Since the task 3.4 partners are also involved in the design of various ASICs built in different CMOS technologies, taking advantages from different emerging NVM technologies, this deliverable is split in three main parts corresponding to the SOT-MRAM whose IP is designed in 40 nm bulk TSMC technology and not used in any use case, and two other technologies whose IPs explore more challenging approaches considered as low TRL: 22FDX + OXRAM/FeFET implemented in the ASICs developed in WP4 and used for different application use cases in WP5.

The first IP presented is designed by **IMEC**. This IP takes advantage of MRAM technology, on top of 40 nm bulk, for storing synaptic weights and processes Analog In Memory Computing (AIMC). This IP includes a 3T1R MRAM storage array, as well as a complete periphery including ADC and DAC to run internally the analog MAC within a digital environment.

The second IP presented is designed by **CEA**. This circuit implements a 22 FDX + OxRAM array that stores multiple values synaptic weights and performs analog matrix-vector multiplications. This array shows an interesting density at cells level, but the high voltage periphery roughly worsens this feature. This has been implemented in a test chip, for silicon measurements.

The third presented IP is designed by **FhG IPMS**. This circuit makes use of the FeFET technology in 22nm FDSOI for storing the synaptic weights in a 1F1R FeFET bitcell configuration to calculate multiply-accumulate (MAC) operations. Hereby, a Flash-like ADC is included as well.