This project has received funding from the Electronic Components and Systems for European Leadership Joint
Undertaking under grant agreement No 876925

ECSEL Joint Undertaking
Electronic Components and Systems for European Leadership

ANDANTE

AI for New Devices And Technologies at the Edge

D3.8 High TRL Technology Foundation IPs characterization results

Deliverable No.	D3.8	**Due Date**	*29-Feb-2024*
Type	Report	**Dissemination Level**	*Confidential*
Version	1.0	**Status**	Final
Description	This deliverable reports the characterization results of high TRL IPs developed within Task 3.4. These IPs are fundamental subcircuits implementing different digital storage functions based on emerging NVM technologies developed in WP2. Each IP is described separately. It should be noted that in ANDANTE, several eNVM technologies are being developed and different design approaches are being explored. .		
Work Package	WP3 – AI building blocks, Methods and Tools.		

Abstract (Published Summary)

This deliverable aims to present the characterization of the high TRL Foundation IPs developed in Task 3.4. These Foundation IPs truly constitute a key point of the ANDANTE project as they constitute a link between emerging NVM technologies, and the neuromorphic architectures designed in WP4. Since memory access consumes a significant portion of energy in neuromorphic applications and the number of parameters becomes larger and larger, the density and energy efficiency of these IPs have a major impact on the overall effectiveness of the integrated circuits in which they are used and their success. of the ANDANTE project.

Since Task 3.4 partners are also involved in the design of various ASICs leveraging different emerging CMOS NVM technologies, this deliverable covers 3 IPs in the following two technologies: 28nm FeFET by FMC and Fraunhofer-IPMS and 22nm OxRAM by CEA .

FMC designed the first IP “an integrated FeFET-based non-volatile memory macroblock with AI acceleration capabilities” presented in this document. This IP takes advantage of FeFET technology to store synaptic weights and processes digital neural network calculations (MAC, pooling, activation function). FMC planned to design a single chip housing both the FeFET-based storage solution and the CMOS digital computing means. However, given that the estimated manufacturing time of the FeFET on 28SLPe was up to 9 months at the time of the macro, the decision was made to minimize the risk of having no results at the end of the project. FMC ultimately opted to build a system consisting of a pre-existing FeFET array storing synaptic weights and an FPGA hosting neural calculations. FMC presents here the resulting board and its results.

CEA designed the second “OxTP” IP presented in this document. This OxTP IP is an all-digital 1024 x 64 bitcell 1T1R memory array based on OxRAM technology integrated with the backend of Global Foundry's 22nm FDX CMOS technology. To challenge the performance of the SRAM 22FDX and in line with the chip philosophy of losing flexibility to improve performance, CEA decided to use this NVM technology as OTP (One-Time Programmable). This IP implements an OxRAM array that stores binarized synaptic weights. This IP was sent to manufacturing within ASIC 2.1, the first pure CMOS version of which is fully effective. ASIC 2.1 version including this NVM-based IP returned from the factory in January 2024. However, these IPs still needed to be packaged and tested. When this deliverable was finalized at the end of May, the packages had not been received and the test results could therefore not be reported in this document.

Fraunhofer IPMS designed the third IP “FeFET based analog in memory computing accelerator GF 28nm SLPE + FeFET) presented in this document. This IP encompasses a FeFET-based crossbar array dedicated to storing weights and facilitating in-memory computing to accelerate neural network applications. This IP is a comprehensive macro that includes not only the requisite analog control circuitry, but also the accompanying digital components necessary for both further processing and testing of the macro elements. This IP constitutes the cornerstone of ASIC 3.1b and thanks to its digital measurement interfaces, used for the characterization of the FeFETs.