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ANDANTE

AI for New Devices And Technologies at the Edge

D3.7 High TRL Technology Foundation IPs implementation

Deliverable No.	D3.7	**Due Date**	*31-Dec-2022*
Type	Report	**Dissemination Level**	*Confidential*
Version	1.0	**Status**	Final
Description	This deliverable reports the design of high TRL IPs developed within Task 3.4. These IPs are fundamental subcircuits implementing synaptic arrays based on emerging NVM technologies developed in WP2. Each IP is separately described. It should be noted that in ANDANTE, several technologies are being developed and different approaches are being explored.		
Work Package	WP3 – AI building blocks, Methods and Tools.		

Abstract (Published Summary)

This deliverable aims at presenting the high TRL Foundation IPs that have been developed under task 3.4. These Foundation IPs really compose a key point of the ANDANTE project as they form a link between the emerging NVM technologies, and the neuromorphic architectures designed in WP4.

As memory access consumes an important part of the energy in neuromorphic applications and as the number of parameters becomes bigger and bigger, the density and power efficiency of these IPs have a major impact on the overall efficiency of ICs and on the success of ANDANTE project.

Since the task 3.4 partners are involved in the design of various ASICs built in different CMOS technologies and taking advantages from different emerging NVM technologies for different use cases, this deliverable is strongly split in two parts corresponding to the two technologies whose IPs are assumed as mature enough to stand in this high TRL deliverable: 22FDX + OXRAM and 28SLPe/22FDX + FeFET.

CEA designed the first IP presented in this document. This IP implements an OxRAM array that stores binarized synaptic weights. This synaptic memory shows a high density, a low energy consumption and a significant throughput.

FMC designed the second IP presented in this document. This IP takes advantage of FeFET technology for storing synaptic weights and processes digital neural network computations (MAC, pooling, activation function). This IP includes a binary FeFET storage array on one side and a digital pure CMOS computational unit on the other side.

FhG developed the third IP based on 28SLPe FeFET- technology. The implementation in 22FDX + FeFET technology is reported in D3.9. The IP reported here implements a FeFET crossbar along with digital and analog periphery for multiply-accumulate operations.