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ANDANTE

AI for New Devices And Technologies at the Edge

D3.6 Foundation IPs specifications

Deliverable No.	D3.6	**Due Date**	*31-May-2021*
Type	Report	**Dissemination Level**	*Confidential*
Version	1.4	**Status**	Final
Description	This deliverable states the specifications for the IP to be developed within Task 3.4. These IP are fundamental subcircuits implementing synaptic arrays based on emerging NVM technologies developed in WP2. Several technologies being developed in ANDANTE and different approaches being explored. Separate specifications are given for each IP.		
Work Package	WP3 – AI building blocks, Methods and Tools.		

Abstract (Published Summary)

This deliverable aims at defining and quantifying key features of each Foundation IP that are developed under tasks 3.4. These Foundations IPs really compose a key point of the ANDANTE project as they form a link between the emerging NVM technologies, and the neuromorphic architectures designed in WP4. As memory access consumes an important part of the energy in neuromorphic applications and as the number of parameters becomes bigger and bigger, the density and power efficiency of these IPs have a major impact on the overall efficiency of ICs and on the success of ANDANTE project.

Since the task 3.4 partners are involved in the design of various ASICs built in different CMOS technologies and taking advantages from different emerging NVM technologies for different use cases, this deliverable is strongly split in three parts. Each part defines the specification for each Foundation IP concerning each of the three selected technologies: 22FDX + OXRAM, 40nm Si Bulk + MRAM, and 22FDX + FeFET.

The first technology to be described and specified is implemented by CEA. The NVM technology called OxRAM is a conductive filament Resistive RAM. This emerging technology is laid in the back end of Global Foundry FDSOI technology: 22 FDX. Two IPs are presented here as two solutions for implementing a fully-connected layer of synapses. The first IP is fully-digital and the OxRAM devices are assumed as binary components; the second IP implements an analog MAC operation considering the same OxRAM devices as multilevel items.

Next part introduces and specifies the IMEC IP which is an analog Matrix-Vector-Multiplication core using MRAM devices laid of a 40 nm bulk CMOS technology. MRAM devices are binary or ternary and the IP includes the computing array, DACs for inputting the incoming data, ADC for extracting the multiplications results and a digital top.

The last technology is developed by a German consortium composed of Fraunhofer Gesellschaft, Friedrich Alexander Universität and Ferroelectric Memory GmbH. Like CEA's OxRAM, the FeFET technology is implemented with GF's 22 FDX technology but the FeFET devices are at the front end level. These components are binaries and are used to perform a convolution between input data and stored data thought 1 bit AND operations.

As these IPs are based on three independent technologies addressing different applications, this document defines the specification for each Foundation IP concerning each of the three selected technologies: FD-SOI 28 nm + OXRAM, 40nm Si Bulk + MRAM, and 22FDX + FeFET