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ANDANTE

AI for New Devices And Technologies at the Edge

D3.10 Low TRL Technology Foundation IPs characterization results

Deliverable No.	D3.10	**Due Date**	*29-Feb-2024*
Type	Report	**Dissemination Level**	*Confidential*
Version	1.0	**Status**	Final
Description	This deliverable reports the characterization results of low TRL IPs developed within Task 3.4. These IPs are fundamental sub-circuits implementing different IP designs of Analog in Memory Computing (AiMC) function based on emerging NVM technologies developed in WP2. It should be noted that in ANDANTE, several eNVM technologies are being developed and different design approaches are being explored. .		
Work Package	WP3 – AI building blocks, Methods and Tools.		

Abstract (Published Summary)

This deliverable aims to present the characterization of low TRL Foundation IPs developed in Task 3.4. These Foundation IPs truly constitute a key point of the ANDANTE project because they constitute a link between emerging NVM technologies, and the neuromorphic architectures designed in WP4. As memory access consumes a significant amount of energy in neuromorphic applications and the number of parameters becomes larger and larger, the density and energy efficiency of these IPs have a major impact on the overall efficiency of ICs where they are used and on the success of the ANDANTE project.

Since Task 3.4 partners are also involved in the design of various ASICs built in different CMOS technologies, leveraging different emerging NVM technologies, this deliverable is divided into three parts corresponding to 40nm SOT-MRAM technology, FDX + 22nm OxRAM and 22nm FDSOI. + FeFET.

In following low TRL IPs, we intend to fully exploit NVM technologies by performing in-memory analog compute vector matrix multiplications. Such use implies great control of the conductance of the devices which is costly to implement. However, inaccuracies in conductance do not prevent sufficiently precise calculations for neuronal applications.

IMEC contributes to the design of a low TRL IP "a matrix vector multiplication core" in Si Bulk 40 nm + MRAM. The initial tape out of the memory resulted in faulty dies on all wafers and several subsequent learning cycles to debug the problem. Therefore, this D3.10 report does not contain basic analog in memory computing (AiMC) characterization reports. However, in the past, IMEC has performed similar characterization of a SOT device fabricated in its factory. The results presented in this report are based on this device which has a difference in electrode configuration and weight manipulation. This device was used to study the operation of matrix vector multiplication (MVM).

CEA contributes to the design of a “low TRL IP analog matrix vector multiplication network” fabricated in 22nm FDX+OXRAM and is fully operational. It demonstrated working analog vector matrix multiplication on a 128 × 128 OxRAM matrix with 3-bit inputs, up to 8 analog levels can be programmed, and scanning of external output currents. Such a level of integration (external output scanning and write verification algorithm) does not make it possible to evaluate the energy efficiency of this approach but at least allows us to assert that the technology can perform such analog MACs operations.

Fraunhofer IPMS contributes to the design of a low TRL IP “analog in memory computing accelerator in “22nm FDSOI based FeFET” fabricated by GF is fully functional. It demonstrated that segments of XF1R bitcells with resistive elements implemented by a series transistor with source degeneration can be a useful implementation for performing analog vector matrix multiplications and its ability to perform analog MAC operations.