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ANDANTE

AI for New Devices And Technologies at the Edge

D3.1 Tools and methodologies specifications

Deliverable No.	D3.1	**Due Date**	*31-Nov-2020*
Type	Report	**Dissemination Level**	*Confidential*
Version	1.0	**Status**	Final
Description	This deliverable provides the specifications for the tools and methodologies to be implemented in Task 3.1 Methods and tools		
Work Package	WP3 – AI building blocks, Methods and Tools.		

Abstract (Published Summary)

This deliverable aims at describing the complete workflows and associated methodologies used by different partners for their design of hardware neural network accelerators developed in ANDANTE. This deliverable defines the tools to be developed in WP3 to facilitate training, simulation, and deployment of neural network models on the targeted HW accelerators. This document covers all the constraints, dependencies, and interfaces for each of the developed tools.

Since we are suffering from the quasi-end of Moore's Law and power consumption is a major issue for many applications in the Edge, new architecture solutions are required to bring lowpower hardware implementing deep neural networks for Edge analytics. Considering that in ANDANTE several designs will be developed by different partners, a common framework for the design of neuromorphic hardware devices and their applications will be developed[1].

The workflow and methodology proposed should make possible to explore different algorithms, architectures and devices for different use cases including the ANDANTE use cases. By covering the full supply chain, it is possible to integrate new results and explore new concepts in an iterative process with an optimal use of resources. Thus, this workflow/methodology needs a multidisciplinary approach to reach the following main objectives:

- Hardware-aware training for the algorithms to provide neuromorphic hardware implementable ANN/SNN solutions.
- Hardware-aware inference for the algorithms to provide neuromorphic hardware able to reach the KPIs targeted by ANDANTE ASICs, platforms and applications.
- Automation of the hardware generation, for ensuring the components quality and decreasing the time-to-market.
- Development of applications in a way that they are not involved in the specifics of the neural network architecture.

[1] Plank, James S., et al. "A unified hardware/software co-design framework for neuromorphic computing devices and applications." 2017 IEEE International Conference on Rebooting Computing (ICRC). IEEE, 2017.