This project has received funding from the Electronic Components and Systems for European Leadership Joint
Undertaking under grant agreement No 876925

ECSEL Joint Undertaking
Electronic Components and Systems for European Leadership

ANDANTE

AI for New Devices And Technologies at the Edge

D2.5 Full flow integration: OxRAM, SOT-MRAM, FeFET

Deliverable No.	D2.5	**Due Date**	*30-May-2022*
Type	Report	**Dissemination Level**	*Confidential*
Version	1.0	**Status**	Final
Description	This deliverable aims to describe the co-integration of emerging Non-Volatile memory (OxRAM, FeFET and SOT-MRAM) with an established logic technology (28nm, 22 FDX and 40nm, respectively), aiming toward Mb arrays demonstration		
Work Package	WP2 – New memory technologies for AI applications.		

PROPRIETARY RIGHTS STATEMENT

This document contains information, which is proprietary to the ANDANTE Consortium.
Neither this document nor the information contained herein shall be used, duplicated or communicated by any means to any party, in whole or in parts, except with prior written consent of the ANDANTE consortium.

Abstract (Published Summary)

In the context of the exploration of new memories for Artificial (with analog compute in-memory) and Spiking Neural Networks, CEA, Imec and Fraunhofer were enabling and demonstrating the scalability of new memory technologies to larger scale AI application for ANN (Artificial Neural Networks).

Three technologies were selected for further demonstration: OxRAM with transistors as select devices, FeFET and SOT-MRAM. Designs of arrays ranging from kb to Mb combining these memory elements with respectively 28nm FDSOI, 22 FDX, and 40nm bulk logic nodes were taped out. For the three technologies, process development has been performed and reported in this deliverable.

CEA developed the process modules for OxRAM co-integration onto the back-end of line (BEOL) part of 28FDSOI front-end transistors. The fabrication of the first 1T1R « pathfinder » lot has been successfully completed allowing the preliminary electrical characterization. Morphological validation has been performed all along process integration, giving insight of process quality. First « healthy » electrical tests allow to validate this new shrank OXRAM cell process integration.

Fraunhofer demonstrated successful memory array implementation using 28nm FeFET and CAM cell realization using FeTFTs. The next step will be to implement memory array using IGZO devices.

IMEC developed the process modules for SOT MRAM co-integration onto the back-end of line (BEOL) part of TSMC wafers with 40nm low power front-end transistors. The pipe cleaner lot of this flow will be used to validate all electrical connections to the devices and have a first read-out of yield.