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ANDANTE

AI for New Devices And Technologies at the Edge

D2.4 Bitcell level device and selector integration

Deliverable No.	D2.4	**Due Date**	*31-May-2021*
Type	Report	**Dissemination Level**	*Confidential*
Version	3.0	**Status**	Final
Description	This deliverable reports the development of memory and selector integration at bitcell level for PCM, OxRAM, SOT-MRAM, FeFET, TFT.		
Work Package	WP2 – New memory technologies for AI applications.		

Abstract (Published Summary)

As part of the Work package 2 dedicated to the enablement of new memory technologies and the demonstration of their scalability and array capacity for larger scale Artificial Intelligence (**AI**) applications, the deliverable 2.4 focus on the bit cell level device and selector integration for Magnetic Random Access Memory (**MRAM**), Ferroelectric Field-Effect Transistor (**FeFET**) based Memory, Oxide Random Access Memory (**OxRAM**) and Phase Change Random Access Memory (**PCRAM**). For these two last types of Resistive Memories (**RRAM**) the report gives a status on the development of materials and their first integration as backend selector associated to these memories in a crossbar array architecture in order to allow implementation of high-density memory.

CEA enabled the integration in a crossbar architecture of resistive memories such as OXRAM and PCRAM by demonstrating a chalcogenide Ovonic Threshold Switch (**OTS**) Backend selector directly fabricated near a RRAM device.

IMEC developed a Spin Orbit Torque Magnetic Memory device capable of <1ns switching in 300mm toolset.

Fraunhofer developed a ferroelectric FET (**FeFET**) with both Si channel and Indium-Gallium-Zinc-Oxide (**IGZO) material**, which opens possibilities to cointegrate this device not only in front-end but also in the backend of line of a logic node.