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ANDANTE

AI for New Devices And Technologies at the Edge

D2.2 Cell layouts for PCM, OxRAM, SOT-MRAM, FeFET

Deliverable No.	D2.2	**Due Date**	*30-Nov-2020*
Type	Report	**Dissemination Level**	*Confidential*
Version	1.0	**Status**	Final
Description	This document summarizes the achievements obtained in the design of cell layouts for PCM, OxRAM, SOT-MRAM, and FeFET carried out by CEA, FhG imec and STC partners and the status of their fabrication..		
Work Package	WP2 – New memory technologies for AI applications.		

Abstract (Published Summary)

The main achievements obtained in tasks 2.1 and 2.2 concerning the design of cell layouts for PCM, OxRAM, SOT-MRAM, FeFET, TFT are summarized as follows:

- **CEA-Leti** in collaboration with STM Crolles developed a new technology generation of both PCM and OXRAM memories considering the application needs and to enable the memory integration into STM 28FDSOI technology (300 mm wafers). Memory cells have been designed including both scaling options and 1S1R integration to demonstrate the scalability of the RRAM technology for large scale AI applications. The CEA-Leti mask set has been ordered and the masks will be delivered during Q1 2021.
- After a phase of stabilization of STM Crolles new route, a full lot (FEOL 28FDSOI MOS selector up to Metal 5) fabrication has been started at STM and will be completed and delivered to CEA-Leti in 20 weeks (scheduled date: March'21). During this stabilization and production phases, M5 short loops fabrication have been also started and will be delivered to CEA-leti in January'21, allowing to start the process module development in CEA-Leti 300mm clean room based on the current MAD 300 route. However, several lithography and patterning steps including scaling options must be completely developed to meet the needs of ANDANTE project.
- **IMEC** has completed a tape out that features an MVMCORE capable of performing 512x256 matrix vector multiplications. This MVMCORE is built from SOT-MRAMbased compute cells. The functionality of the array has been verified in circuit simulations. As a next step, the FEOL is expected back from foundry in 2021. Thereafter, imec will start processing BEOL+MRAM layers and this is expected to finish in early 2022.
- **Fraunhofer** and FMC developed FeFET based NVM arrays and crossbars, which are suitable for analog In-Memory Computing based on the currently developed 28SLP technologies from GLOBALFOUNDRIES. • The mini-array test structure for 22FDX (earlier version) is currently running in GLOBALFOUNDRIES dedicated for process optimization and experimental data to supply for the model generation. Furthermore, arrays and crossbars are currently running in GLOBALFOUNDRIES 28SLP technology.