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Early Power Extraction with Cadence® Tools

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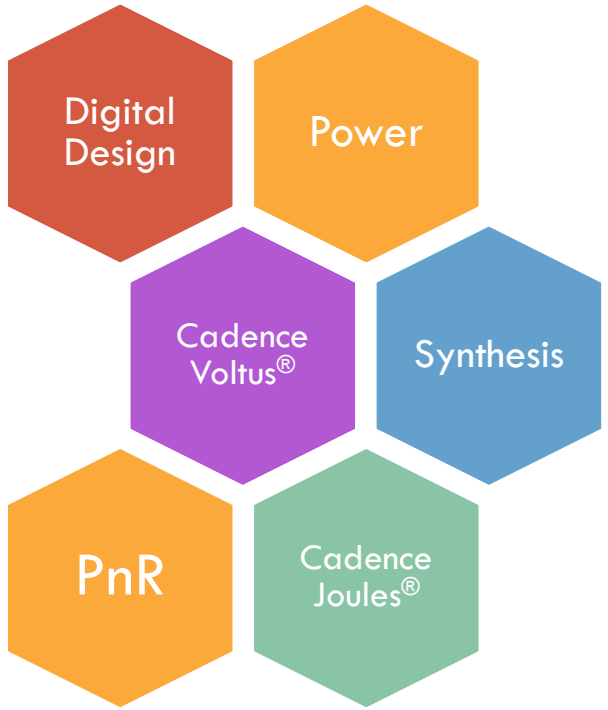
OUTLINE

- Overview of Power Extraction
- Challenges and Opportunities
- Early Power Extraction with Cadence Joules®
- Results

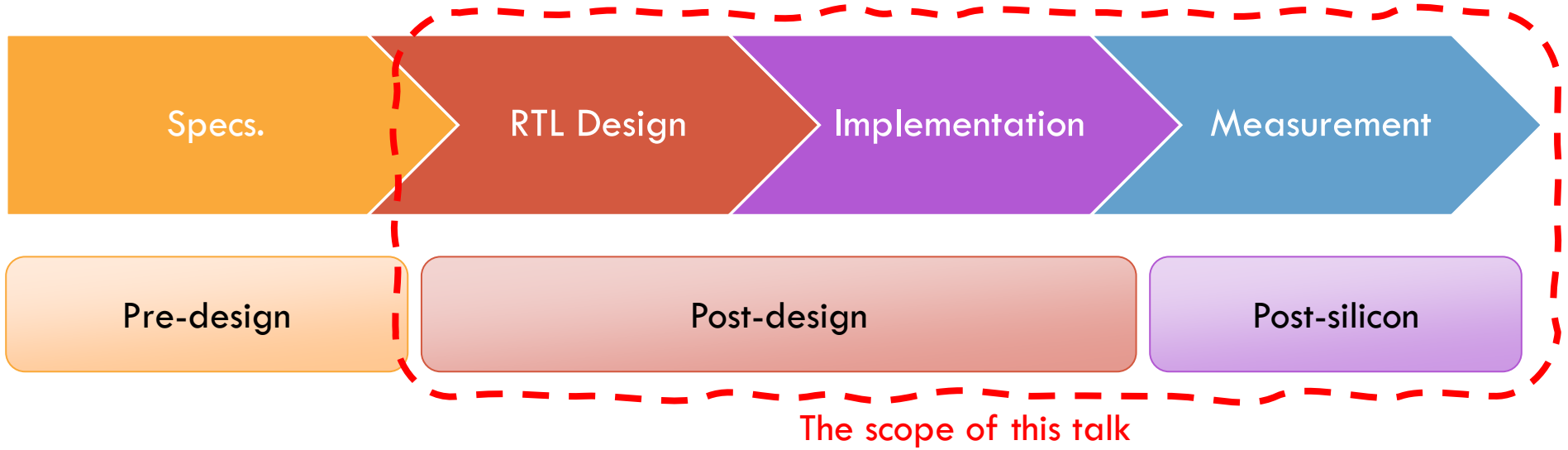
Keywords



Disclaimer: the following slides aim to provide an honest review of Cadence power extraction flows.

OVERVIEW OF POWER EXTRACTION

- Estimation of **power consumption** before actual silicon measurement
- Challenges
  - Accuracy compared with measurement
  - Consistency across the design phase



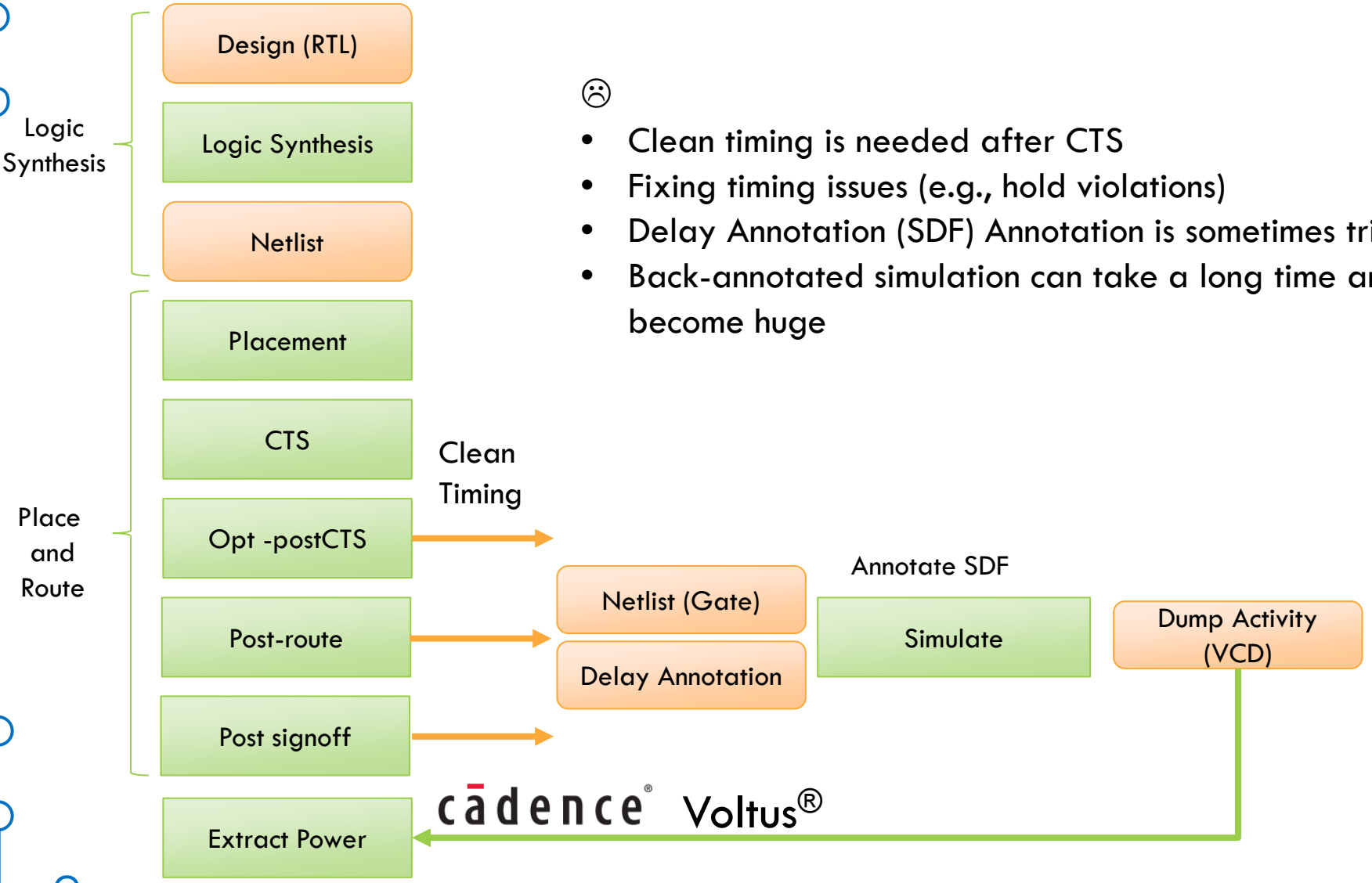
TERMINOLOGY

- VCD: Value Change Dump ➔ Record activities chronologically
- TCF: Toggle Count Format ➔ Probabilistic activity and toggle rate
- SDF: Standard Delay Format

POWER EXTRACTION APPROACHES

- **S) Standard** Power Extraction Flow
- **P) Probabilistic** Power Extraction (X% Switching Activity)
- **E) Early** Power Extraction Flow

S) STANDARD POWER EXTRACTION FLOW



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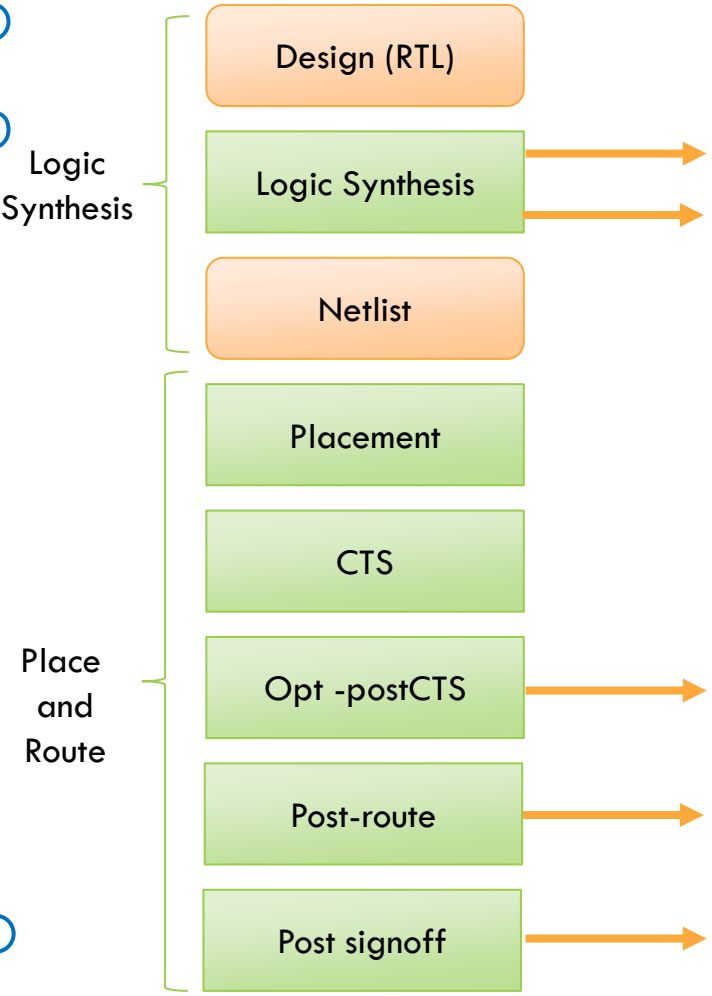
- Clean timing is needed after CTS
- Fixing timing issues (e.g., hold violations)
- Delay Annotation (SDF) Annotation is sometimes tricky
- Back-annotated simulation can take a long time and VCD can become huge

P) X% SWITCHING ACTIVITY



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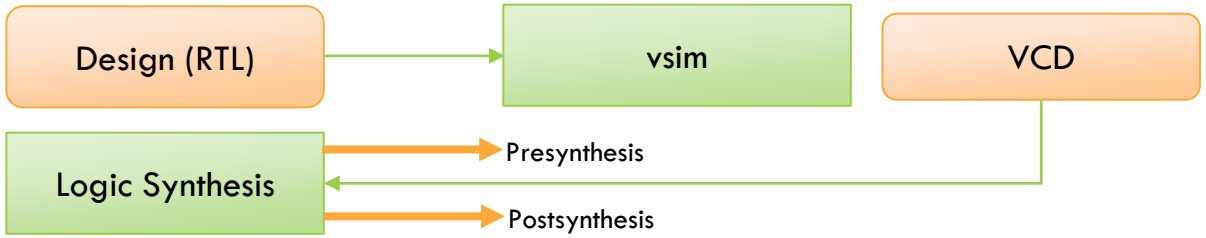
- Very fast and independent of simulation
- Always available in synthesis and PnR tools (report_power)

☹

- Not representative on its own
- Unless we run the standard power estimation and correlated the activity

- Default activity of the tools: 20%
- Most of the cases too pessimistic

E) EARLY POWER EXTRACTION FLOW (E1)



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- Clean timing is NOT mandatory
- No need to fix timing issues
- No need for SDF annotation
- RTL VCD generation is much faster and VCD is smaller

😐

- Accuracy? ➔ See next slides
- Use the newly integrated tool: Cadence Joules®

cadence®

Joules RTL Power Solution

Unified power calculator for accurate RTL power and signoff-quality gate power

https://www.cadence.com/en_US/home/tools/digital-design-and-signoff/power-analysis/joules-rtl-power-solution.html

CADENCE JOULES® RTL POWER SOLUTION

- Integrated within Genus® Synthesis Solutions
- Claims:
  - RTL within 15% of signoff power
  - Up to 20X faster time-based power analysis
  - Bridge between verification, implementation and signoff
  - Direct integration with **Palladium platform** for quick peak power identification

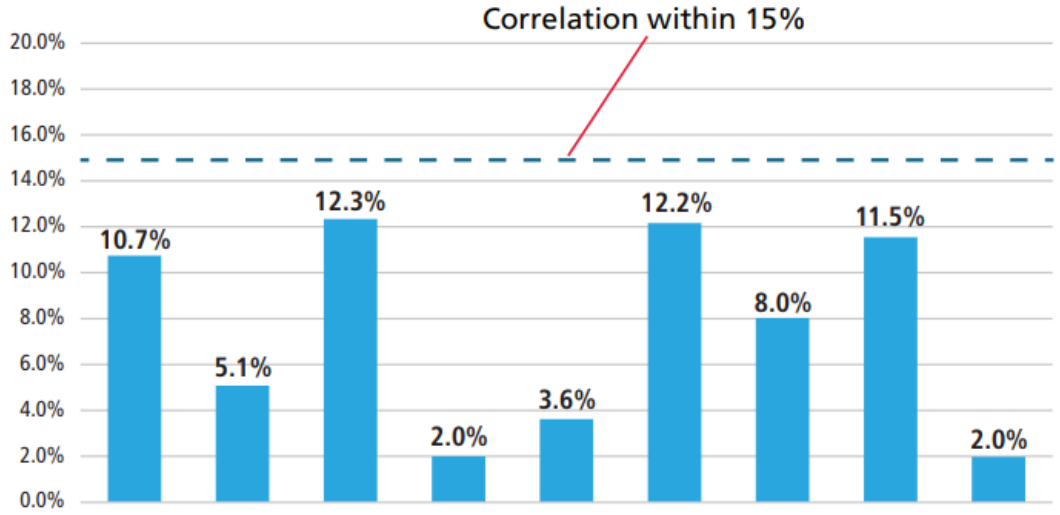
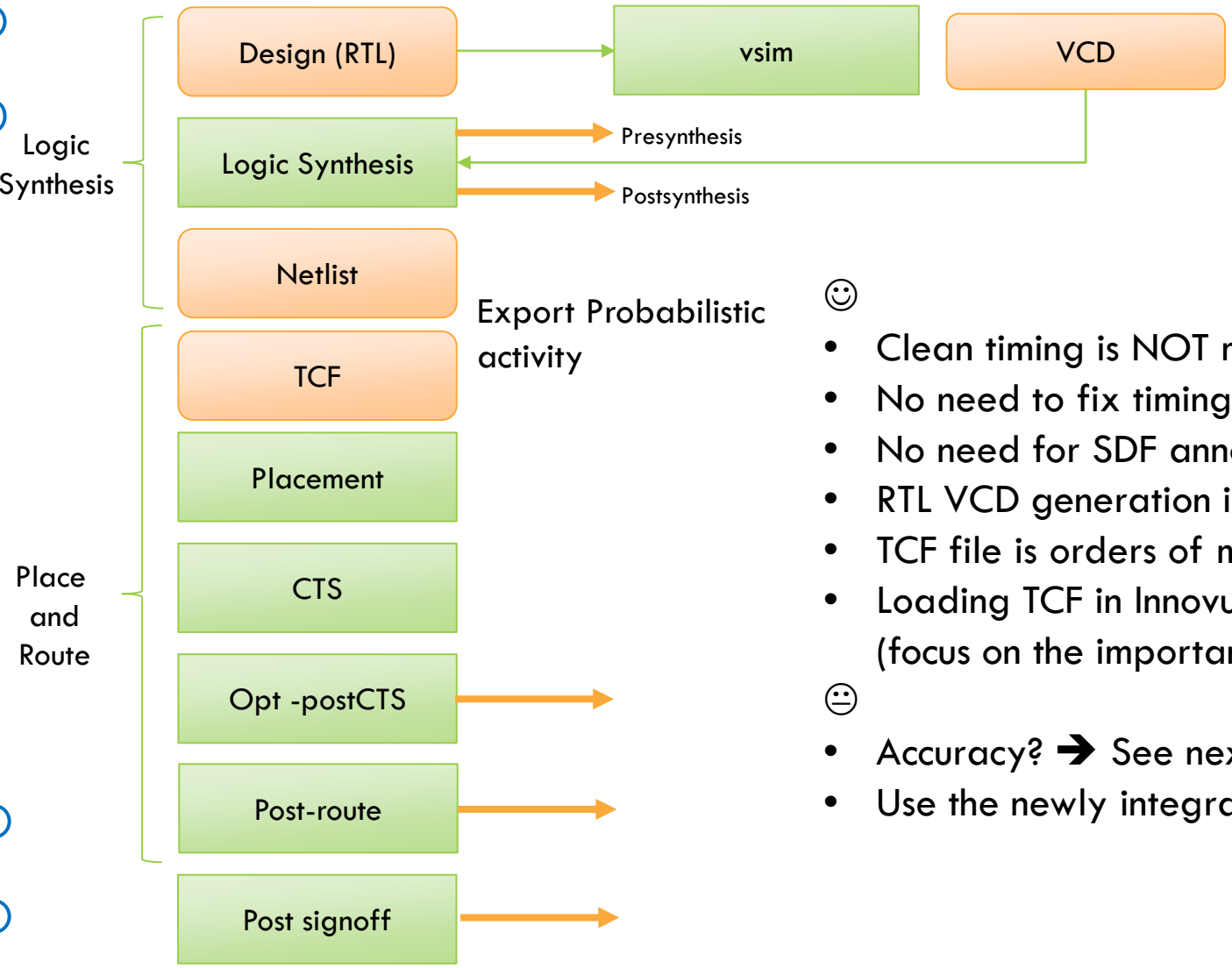


Figure 1: Joules RTL Power Solution correlation to Voltus signoff power across real customer designs

https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/tools/digital-design-signoff/joules-rtl-power-solution-ds.pdf

E) EARLY POWER EXTRACTION FLOW (E2)



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- Clean timing is NOT mandatory
- No need to fix timing issues
- No need for SDF annotation
- RTL VCD generation is much faster and VCD is smaller
- TCF file is orders of magnitude smaller than VCD
- Loading TCF in Innovus allows it to optimize power better (focus on the important parts of the design)

😐

- Accuracy? ➔ See next slides
- Use the newly integrated tool: Joules

EXPERIMENTAL SETUP

Scenario	Application	Design	Node (nm)
A	Coremark	RISC-V	22
B	Dhrystone	RISC-V	22
C	Tree Traversal	RISC-V + Accelerator	22
D	Brain Signal Acquisition	ASIP	180

Operating conditions are kept constant in each scenario

PROBABILISTIC POWER EXTRACTION

Pwr. Engine	Phase	Power Extract.	|Error%| A
Joules	Post-synthesis	P	124%
Voltus	Post-signoff	P	373%
Voltus	Post-signoff	S	Baseline

Probabilistic power extraction can be very inaccurate if activity is non-uniform
Also, it is not consistent across different steps

ACTIVITY-BASED POWER EXTRACTION

- Design (RTL)
- Pre-synthesis
- Generic
- Map
- Incr
- Export
- Synthesis Netlist
- Placement
- Early Global Route
- CTS
- Opt – Post CTS
- Routing
- Opt - Post Route
- Signoff

			|Error%|			
Pwr. Engine	**Phase**	**Power Extract.**	**A**	**B**	**C**	**D**
Joules	Pre-synthesis	E1	29%	-	-	-
Joules	Post-synthesis	E1	25%	26%	28%	19%
Legacy*	Post-synthesis	E1	36%	-	-	-
Voltus	Post-place	S	16%	-	-	-
Voltus	Post-CTS hold opt	S	5%	-	-	-
Voltus	Post-route	S	3%	-	-	-
Voltus	Post-signoff	E2	12%	15%	9%	7%
Voltus	Post-signoff	S	Baseline			

- : Not measured

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- Design (RTL)
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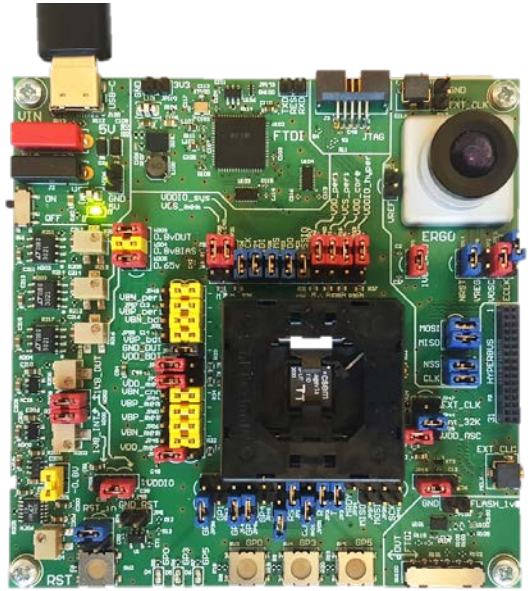
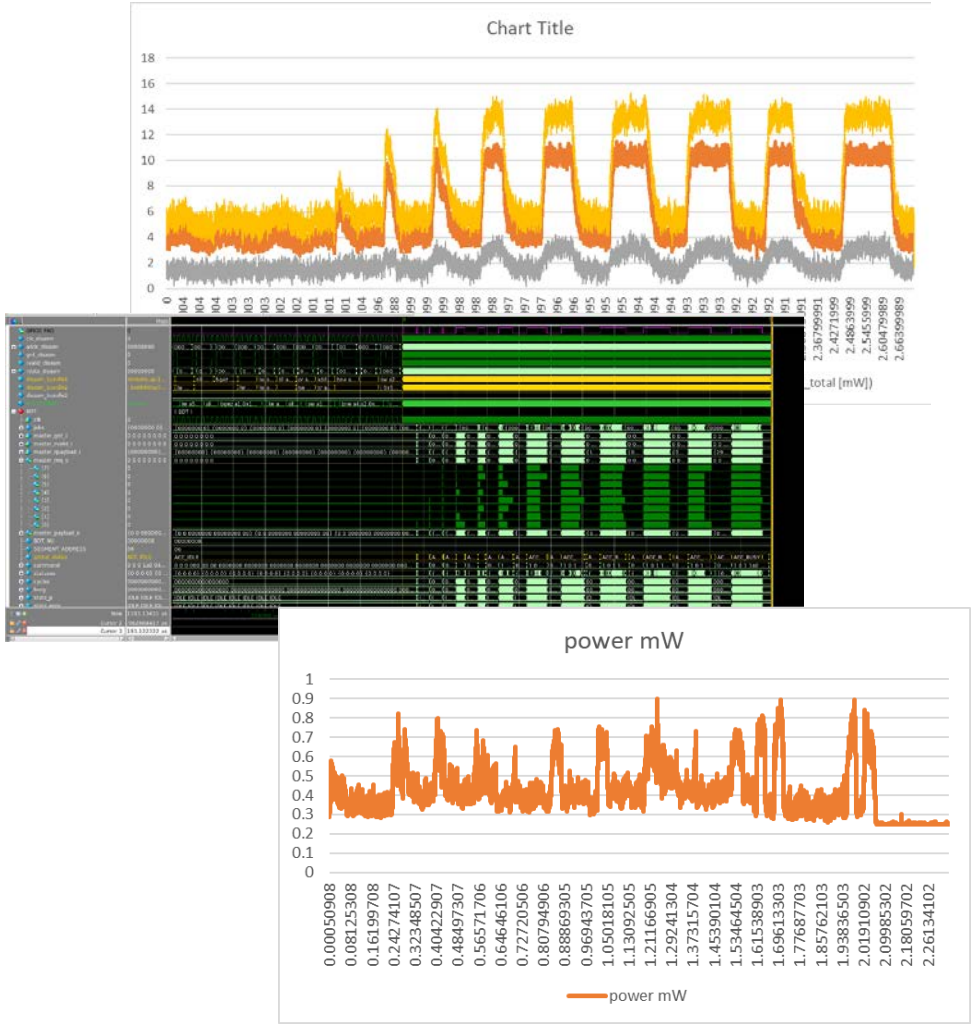
SILICON MEASUREMENT

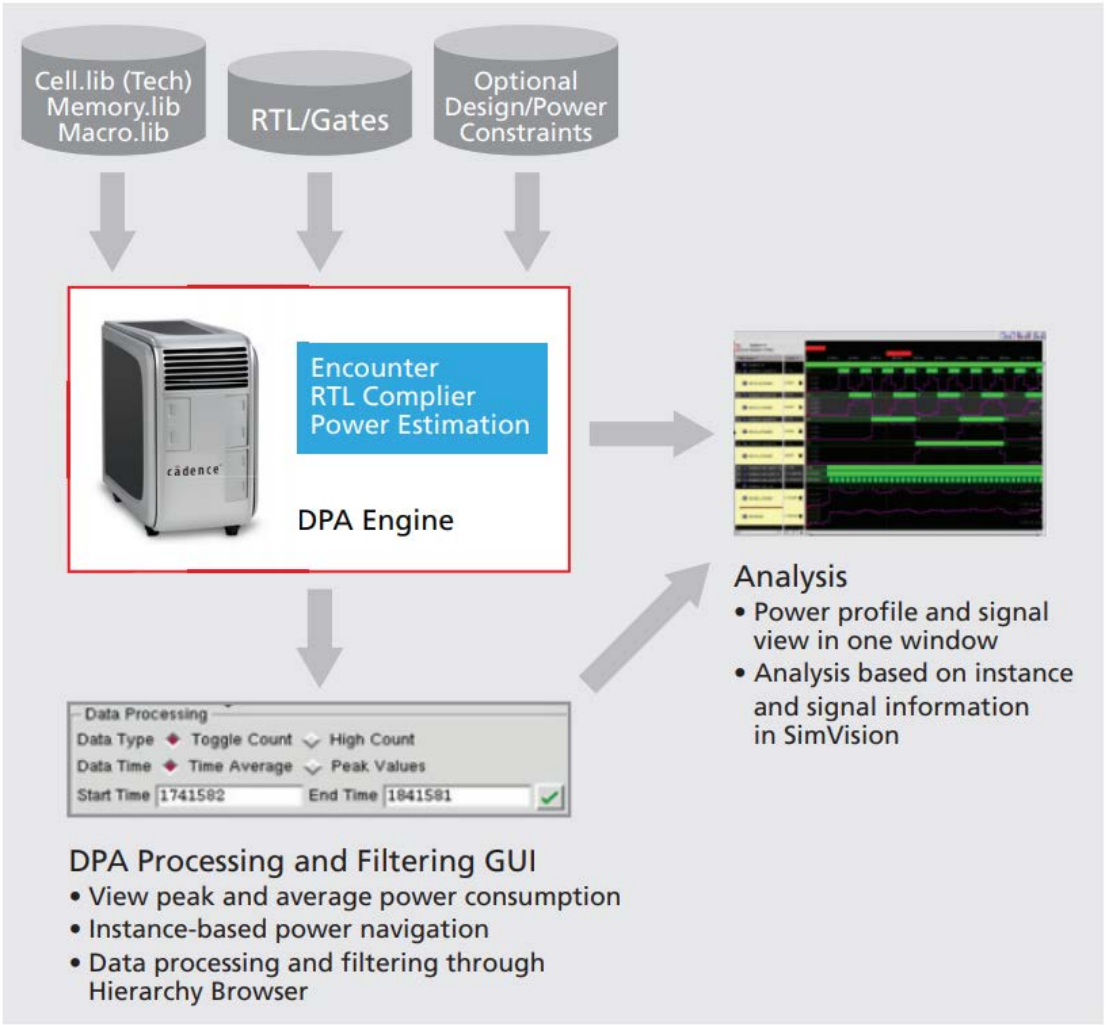




Measurements match Standard Power Extraction within 5% of error

DYNAMIC POWER ANALYSIS (DPA) WITH CADENCE© PALLADIUM©

- Dynamic Power Analysis
- Emulation based verification
- Joules ➔ Palladium



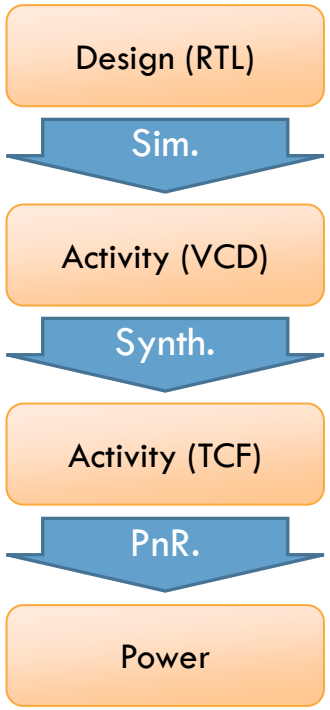
https://www.cadence.com/en_US/home/tools/system-design-and-verification/emulation-and-prototyping/palladium.html

SUMMARY

- **S) Standard** Power Extraction Flow
  - The accurate and consistent approach
- **P) Probabilistic** Power Extraction (X% Switching Activity)
  - Not reliable
- **E1) Early** Power Extraction Flow (error up to 30%)
  - Faster but still accurate

SUMMARY

- **E2) Early** Power Extraction Flow (error up to 15%)
  - Trustable and accurate results
  - Allow for activity-aware power optimization
  - Consistent across the PnR flow



THANK YOU!