ANDANTE

Design and Implementation of Neuromorphic ASICs and Platforms for Edge Computing Application Solutions

ANDANTE

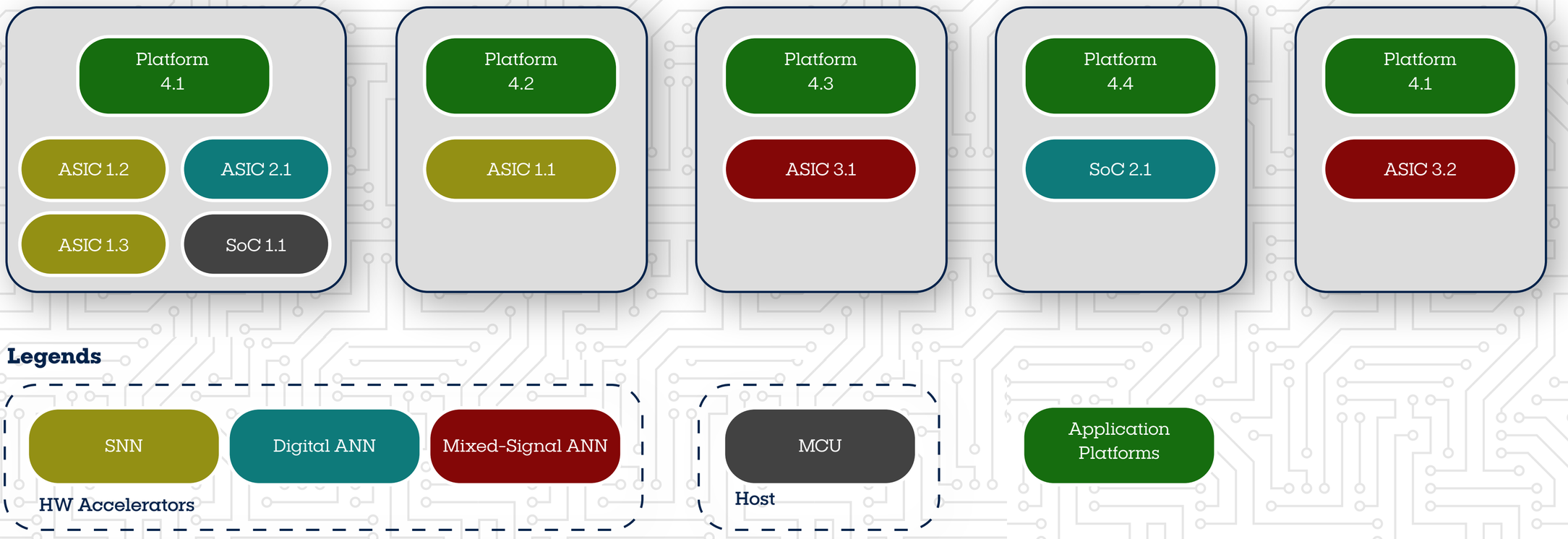
Objectives

- Design of neuromorphic accelerators (ANN and SNN) for edge computing solutions
- Validation of accelerators in dedicated platforms for various applications domains
- Evaluation of platforms and accelerators performances through realistic use cases

Hardware Challenges

- Managing the complexity of different ASIC design technologies
- Integration of neuromorphic accelerators and sensors for various applications in the same platform
- Achieving high energy-efficiency

Main Components and Platforms for efficient Edge computing Solutions



Neuromorphic Accelerators for Edge Computing Solutions

AI Components	ANDANTE ID	Description	Technology	Design Owner
Mixed-signal **SNN**	**ASIC 1.1**	Multi-ASIC for exploration of parallelized and distributed SNN algorithms	28 nm CMOS	Infineon
Mixed-signal **SNN**	**ASIC 1.2**	Multi-core targeting low-dimensional signal representations, such as auditory signals, vibrations, or bio-signals not related to machine vision	28 nm FDSOI	University of Zurich
Front-end	**ASIC 1.3**	Audio front-end performing acoustic inference sensing tasks: acoustic feature extraction (AFE) and classification	40 nm	SynSense
Digital **ANN**	**ASIC 2.1**	Feature extractor circuit to address image classification, segmentation and detection applications	22nm FDX	CEA
Digital **CNN**	**SoC 2.1**	Neural Compute Engine (NCE) targeting NN acceleration for smart vision applications in digital life domain	22nm FDX	CSEM
Mixed-signal **ANN**	**ASIC 3.1**	Inference accelerator with a multi-core architecture using analog in-memory computing; targeting voice activity detection (VAD)	22nm FDX	Fraunhofer
Mixed-signal **ANN**	**ASIC 3.2**	Analogue neuronal network (aNN) for tinyML applications. To be evaluated in the context of one-key-word-spotting for a limited amount of accents	28nm CMOS with RRAM	Infineon
MCU	**Soc 1.1**	Microcontroller STM32 aiming to identify best tradeoff between SoC features and functionality, having a direct impact on the silicon area and final cost	28 nm or lower	STMicroelectronics

Evaluation Platforms for Various Edge Computing Applications

Platform/ board	Short Description	Associated Components	Associated Domains and Use Cases	Contributors
4.1	STM32-based hybrid neuromorphic platform combining SNN and ANN ASICs to perform complementary and efficiently AI features. Designed to support a variety applications in digital farming, transport and smart mobility, and digital life domains	SoC 1.1, ASIC 1.2, ASIC 1.3 ASIC 2.1	**Digital Farming:** UC2.1, UC2.2 **Transport and Smart Mobility:** UC3.1, UC3.2, UC3.3, UC3.4 **Digital life:** UC5.1, UC5.2	CEA, STMicroelectronics, SynSense, Televes, University of Zurich
4.2	A Spiking Neural Microcontroller (SNMC) platform intended, for instance, for radar/optical sensor applications	ASIC 1.1	**Digital Industry:** UC1.1 **Healthcare:** UC4.3	Infineon
4.3	Includes a mixed-signal ASIC and controller/peripheral units, suitable for instance for voice activity detection	ASIC 3.1	**Digital Industry:** UC1.1 **Digital life:** UC5.1.4	Fraunhofer
4.4	Provides effective interface between SynSense accelerator and the event-based camera with low latency and low power consumption for vision-based human-computer interaction	SoC 2.1	**Digital life:** UC5.2	CSEM, SynSense
Board 4.1	An Analog Neuronal Network Microcontroller (ANMC) board; only intended for the evaluation of ANN ASICs	ASIC 3.2	**Digital life:** UC 5.1.5	Infineon

Main first year achievements

- ASIC and platform requirement specifications based on use case needs
- High-level design specifications

Next Steps

Mid-term

- Detailed design specifications
- Implementation of ASICs, SoCs and platforms

Long-term

- Validation of hardware (ASICs, SoCs and platforms)
- Integration of tools and software in the HW platforms in collaboration with WP3
- Delivery of hardware platforms to WP5 for use cases implementation