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Design of Neuromorphic ASICs and Platforms for Edge Computing

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Objectives

- Design of neuromorphic hardware: inference accelerators based on analog, digital and spiking neurons
- Design dedicated platforms for 5 application domains integrating the neuromorphic IP cores (ASICs, SoCs)
- Integrate and test the platforms and accelerators for their performance evaluation through 14 use cases

Challenges

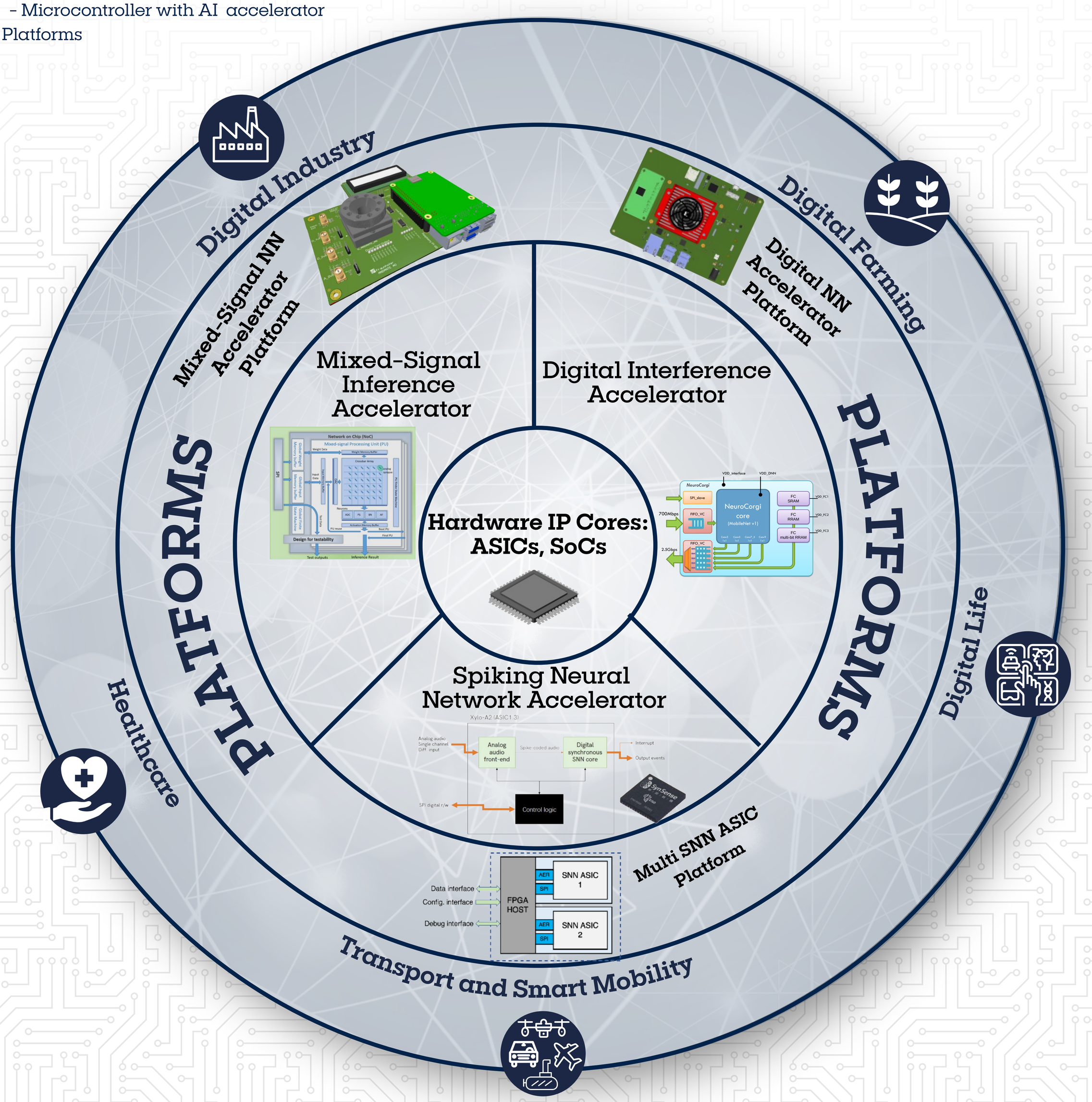
- 8 Design ASICS
  - 2 SNN ASICs
  - 2 Digital inference accelerators
  - 3 Mixed-signal inference accelerators with in-memory computing
  - Microcontroller with AI accelerator
- 6 Platforms

Challenges

- Managing design complexity and several design types (digital, mixed-signal with analog in-memory computing) of a wide range of technologies down to 22 nm
- HW/SW co-design of neuromorphic hardware
- HW/SW integration and test of neuromorphic accelerators and sensors for various applications in the same platform

Benefits

- High energy efficiency
- Low latency
- Data privacy
- High integration



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AI for New Devices And Technologies at the Edge

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"This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement № 876925. The JU receives support from the European Union's Horizon 2020 research and innovation programme and France, Belgium, Germany, Netherlands, Portugal, Spain and Switzerland"

ECSEL Joint Undertaking
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